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SPECIFICATION

VXT340MQIA-01

☐ Preliminary Specification

☐ Final Specification

Approved By:
Date:

2. Revision Record

Date	Rev.No.	Page	Revision Items	Prepared
2023-05-31	**V00**		**The first release**	**Solon**
2024-02-23	**V01**		**Add Quality Assurance**	**Solon**

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3. General Specifications

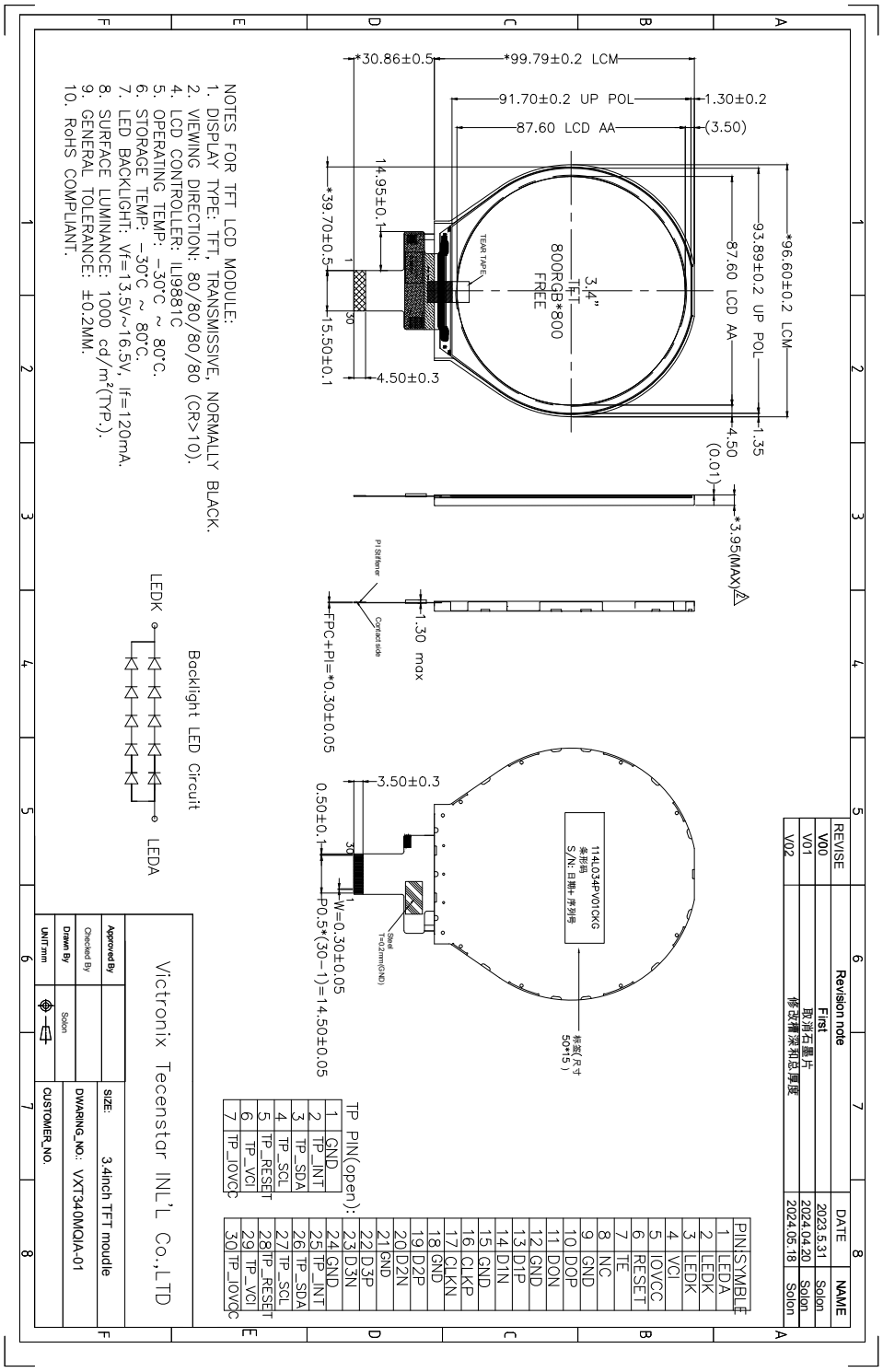
VXT340MQIA-01 is a TFT-LCD module. It is composed of a TFT-LCD panel, driver IC, FPC, a back light unit. The3.4'' display area contains 800x (RGB)x 800 pixels and can display up to 16.7M colors. This product accords with ROHS environmental Criterion.

Item	Contents	Unit	Note
LCD Type	TFT	-	
Display color	16.7M	-	1
Viewing Direction	ALL	O'Clock	
Operating temperature	-30~+80	℃	
Storage temperature	-30~+80	℃	
Module size	Refer to outline drawing	mm	2
Active Area(W×H)	87.6X87.6	mm	
Number of Dots	800（RGB）X800	dots	
TFT Driver IC	ILI9881C	-	
Power Supply Voltage	2.8	V	
Backlight	5S2P-LEDs	pcs	
Weight	---	g	
Interface	MIPI	-	

Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: Without FPC and Solder.

4.Outline Drawing



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5. Absolute Maximum Ratings(Ta=25℃)

5.1 Electrical Absolute Maximum Ratings.(Vss=0V ,Ta=25℃)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VCI	-0.3	6.5	V	1，2
Power Supply Voltage	IOVCC	-0.3	3.3	V	1，2

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.

2. $V_{CI} > V_{SS}$ must be maintained.

3. Please be sure users are grounded when handing LCD Module.

5.2 Environmental Absolute Maximum Ratings.

Item	Storage		Operating		Note
	MIN.	MAX.	MIN.	MAX.	
Ambient Temperature	-30℃	80℃	-30℃	80℃	1,2
Humidity	-	-	-	-	3

1. The response time will become lower when operated at low temperature.

2. Background color changes slightly depending on ambient temperature.

   The phenomenon is reversible.

3. Ta<=40℃:85%RH MAX.

   Ta>=40℃:Absolute humidity must be lower than the humidity of 85%RH at 40℃.

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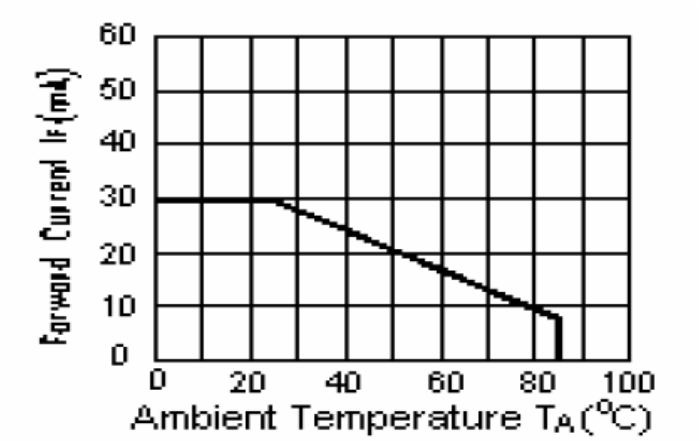
6. Electrical Specifications

6.1 Electrical characteristics(Vss=0V ,Ta=25℃)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Analog Power supply		VCI	Ta=25℃	2.5	2.8	6.0	V	
Digital Power supply		IOVCC	Ta=25℃	1.75	2.8	3.3		
Input voltage	'H'	V_{IH}	Ta=25℃	0.7*IOVCC	-	IOVCC	V	
	'L'	V_{IL}	Ta=25℃	0	-	0.3*IOVCC	V	

6.2 LED backlight specification(VSS=0V ,Ta=25℃)

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply voltage	Vf	If=120mA	13.5	15	16.5	V	
Uniformity	∆Bp	If=120mA	75	-	-	%	
Life Time	time	If=120mA	20K	30K	-	hours	1



Note 1: Brightness to be decreased to 50% of the initial value at ambient temperature TA=25℃

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6.3 Interface signals

Pin No.	Symbol	I/O	Function	Note
1	LEDA	P	LED back light(Anode).	
2-3	LEDK	P	LED back light(Cathode).	
4	VCI	P	Analog Power supply	
5	IOVCC	P	Digital Power supply	
6	RESET	I	Reset pin, Active Low.	
7	TE	O	Tearing effect output pin	
7	GND	P	Ground.	
8	NC	-	NO connect.	
9	GND	P	Ground.	
10	D0P	I	MIPI differential data0+ input.	
11	D0N	I	MIPI differential data0- input.	
12	GND	P	Ground.	
13	D1P	I	MIPI differential data1+ input.	
14	D1N	I	MIPI differential data1- input.	
15	GND	P	Ground.	
16	CLKP	I	MIPI CLOCK+differential signal input .	
17	CLKN	I	MIPI CLOCK- differential signal input.	
18	GND	P	Ground.	
19	D2P	I	MIPI differential data2+ input.	
20	D2N	I	MIPI differential data2- input.	
21	GND	P	Ground.	
22	D3P	I	MIPI differential data3+ input.	
23	D3N	I	MIPI differential data3-input.	
24	GND	P	Ground.	
25	TP_INT	-	NO connect.	
26	TP_SDA	-	NO connect.	
27	TP_SCL	-	NO connect.	
28	TP_RESET	-	NO connect.	
29	TP_VCI	-	NO connect.	
30	TP_IOVCC	-	NO connect.	

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6.4 AC Characteristics

6.4.1 DSI Timing Characteristics

6.4.1.1 High Speed Mode-Clock Channel Timing

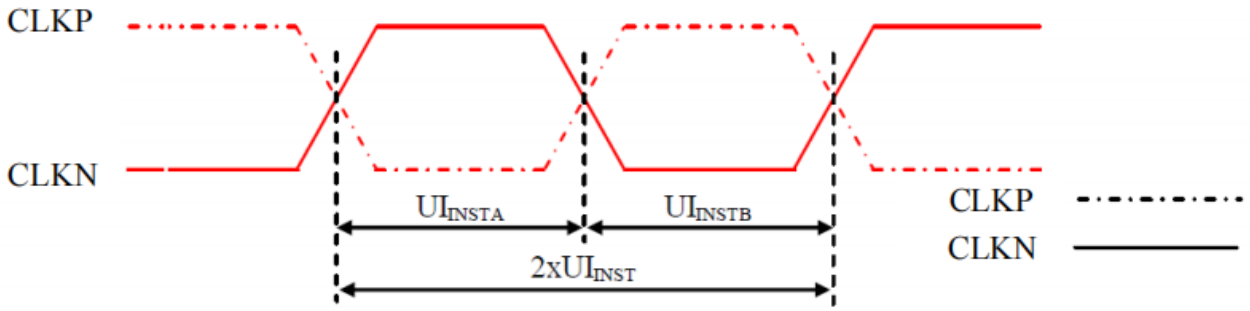

Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

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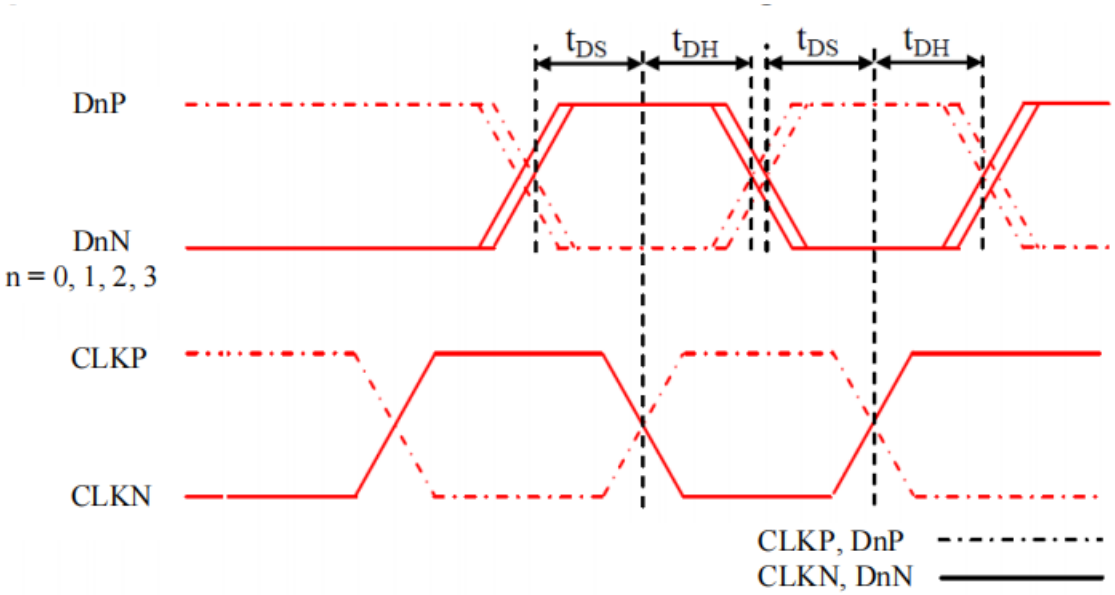
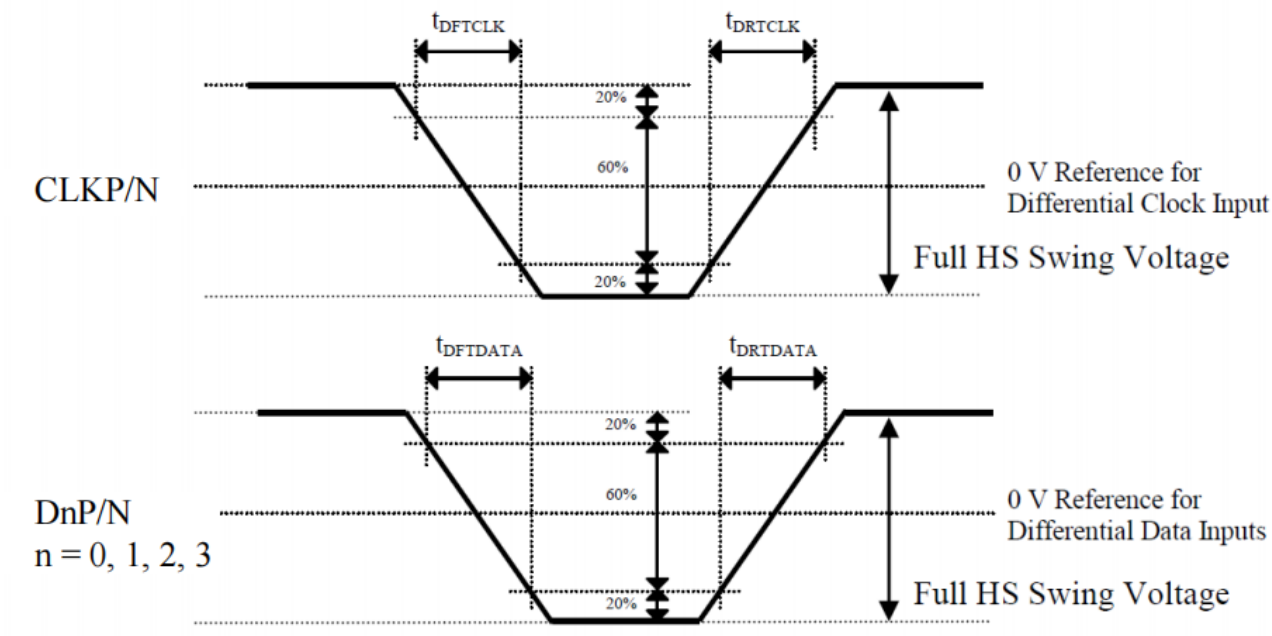
6.4.1.2 High Speed Mode-Data Clock Channel Timing



Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

6.4.1.3 High Speed Mode-Rising and Falling Timings



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Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

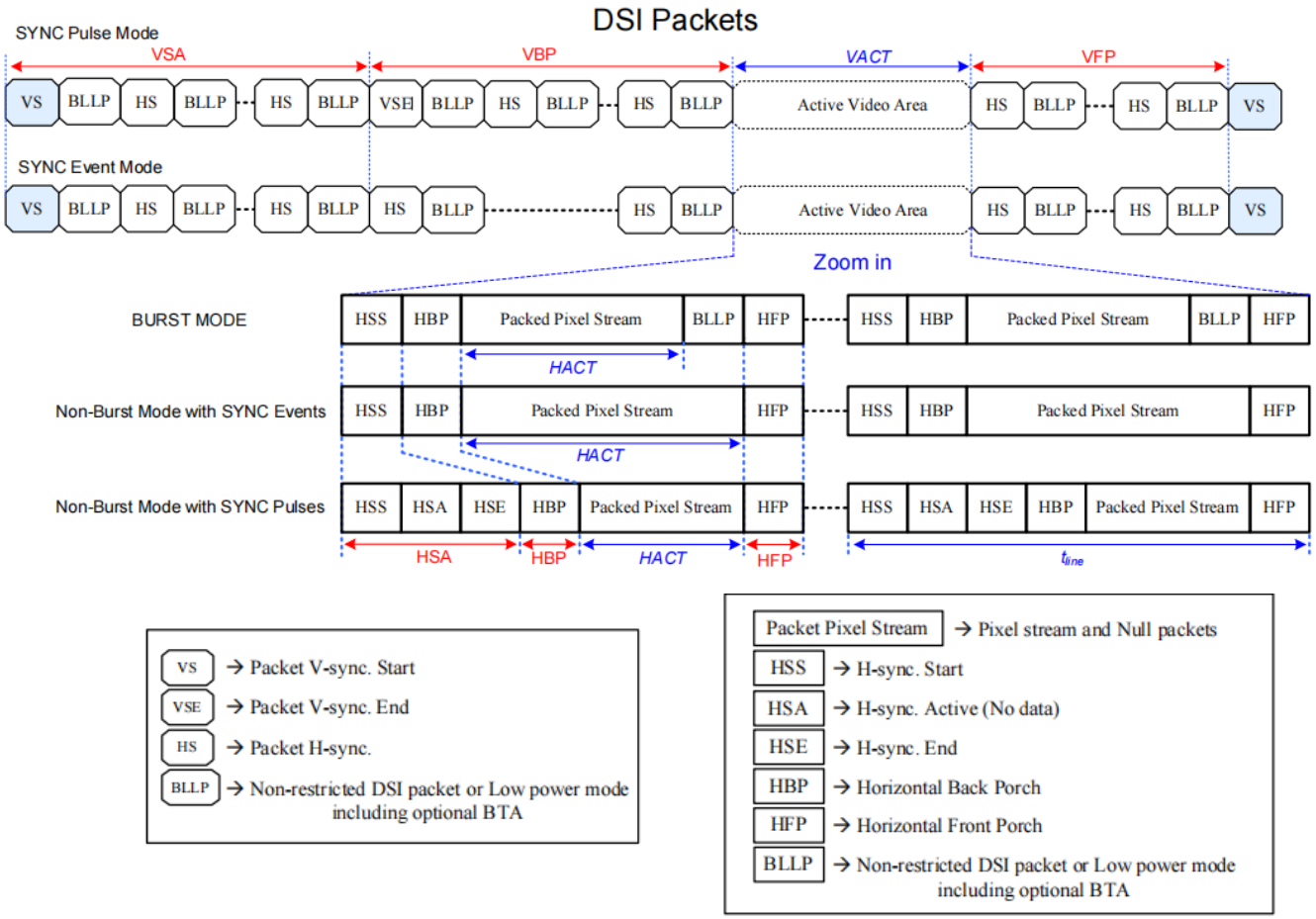
6.4.1.4 Low Speed Mode - Bus Turn Around

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

6.4.1.5 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	TBD	TBD	-	Line
Vertical Back Porch	VBP	TBD	TBD	-	Line
Vertical Front Porch	VFP	TBD	TBD	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	TBD	TBD	-	Pixel
Horizontal Back Porch	HBP	TBD	TBD	-	Pixel
Horizontal Front Porch	HFP	TBD	TBD	-	Pixel
Active pixels per line	HACT	-	800	-	Pixel
Line time	t_{line}	TBD		-	bps/lane
Bit rate	BR_{bps}	200		Note 5	Line

1 UI=1/Bit rate

HAS(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”

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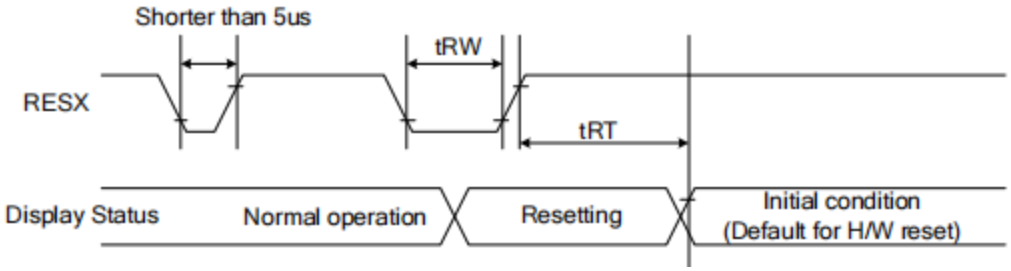
6.4.2 Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

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Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

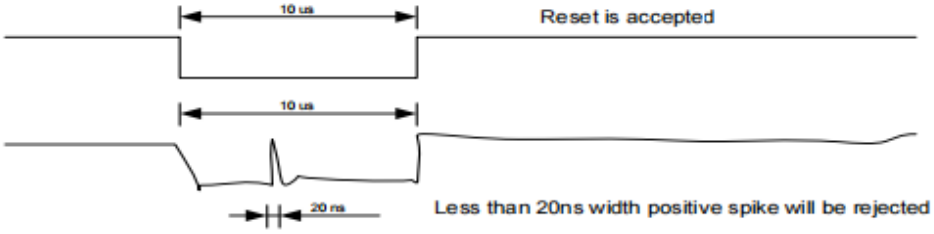


Figure 125: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. Optical Characteristics

Item	Symbol	**Condition**	Min.	Typ.	Max.	Unit	Note
Brightness	Bp	θ=0° Φ=0°	800	1000	-	Cd/m^2	1
Uniformity	⊿Bp		75	-	-	%	1,2
Viewing Angle	3:00	Cr≥10	-	85	-	Deg	3
	6:00		-	85	-		
	9:00		-	85	-		
	12:00		-	85	-		

Contrast Ratio	Cr		θ=0° Φ=0°	1000	1200	-	-	4
Response Time	$T_{r+}T_f$			-	30	35	ms	5
Color of CIE Coordinate	W	x	θ=0° Φ=0°	Typ -0.05	0.322	Typ +0.05	-	1,6
		y			0.342		-	
	R	x			0.661		-	
		y			0.323		-	
	G	x			0.274		-	
		y			0.593		-	
	B	x			0.134		-	
		y			0.124		-	
NTSC Ratio	S			-	70	-	%	

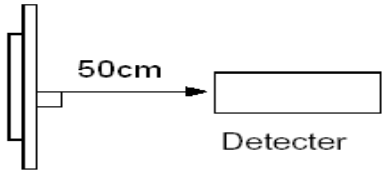
Note：The parameter is slightly changed by temperature, driving voltage and materiel

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment BM-7 (Φ5mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.



Note 2: The luminance uniformity is calculated by using following formula.

⊿Bp = Bp (Min.) / Bp (Max.)×100 (%)

Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.

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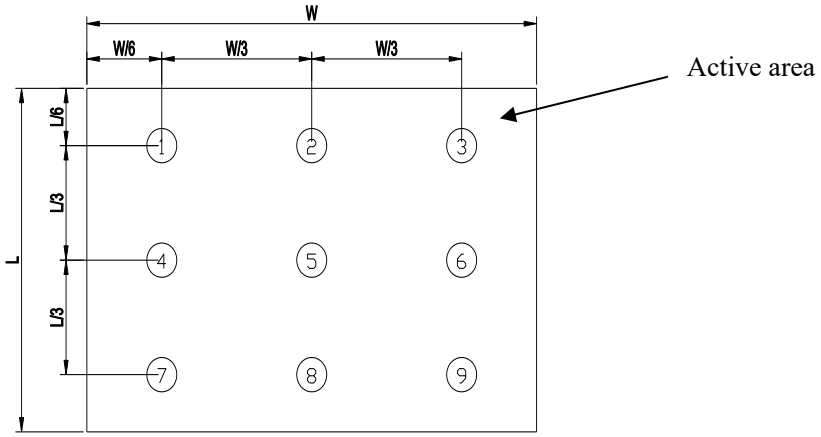
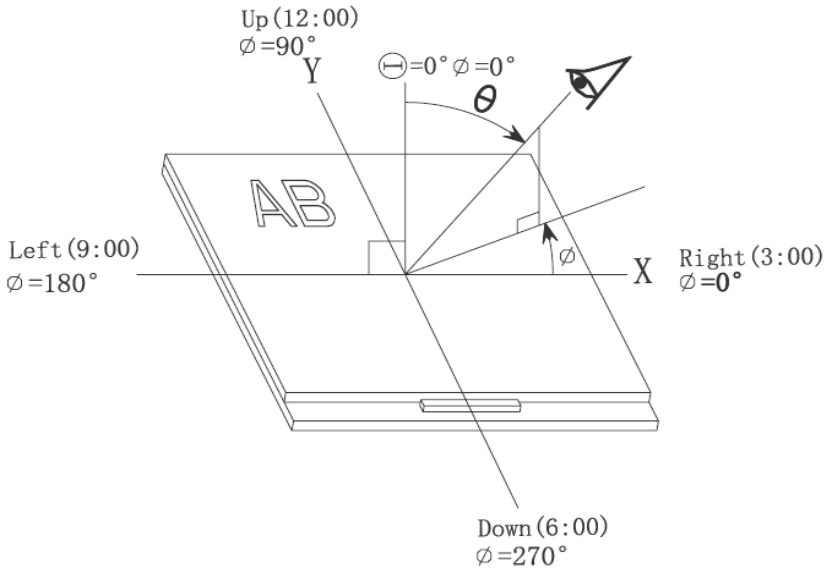
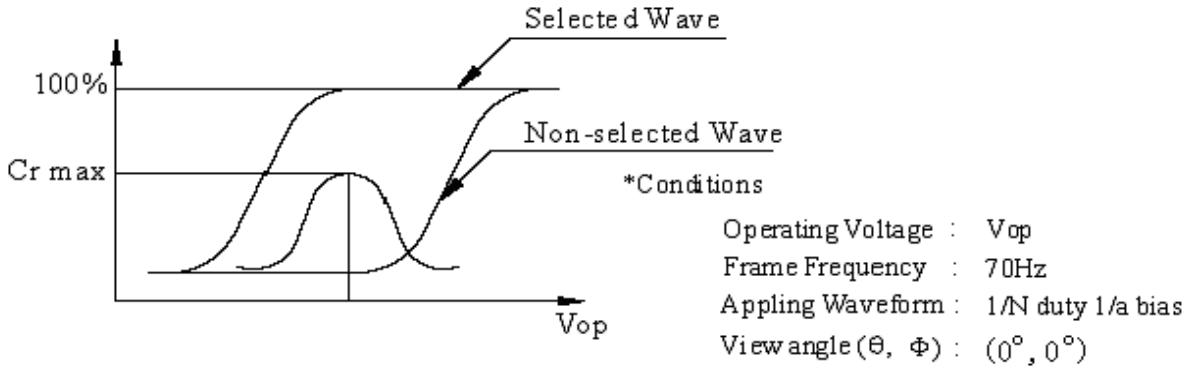


Note 3: The definition of viewing angle:

Refer to the graph below marked by θ and Φ



Note 4: Definition of contrast ratio.(Test LCD using DMS501)



$$Contrast\ ratio(Cr) = \frac{Brightness\ of\ selected\ dots}{Brightness\ of\ non-selected\ dots}$$

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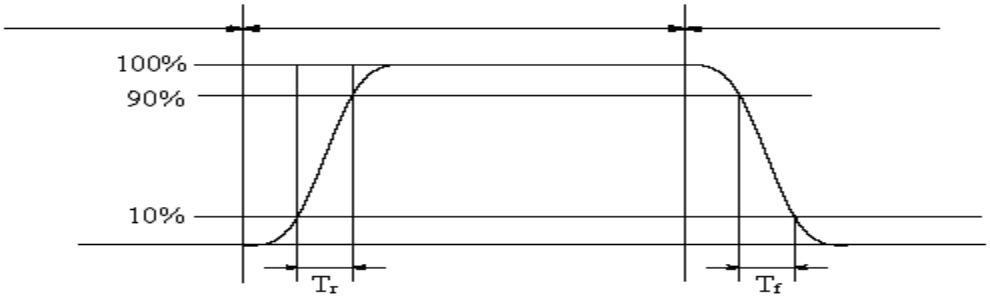
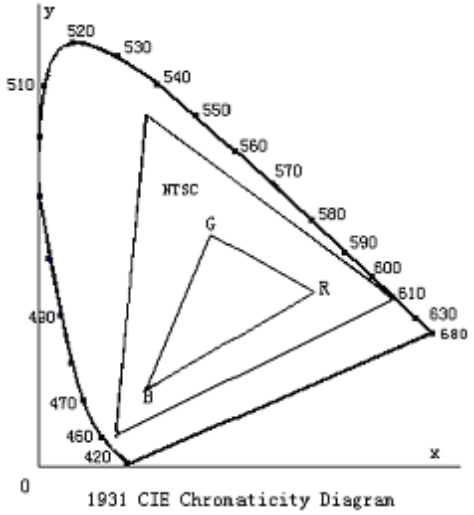
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from“black”to“white”(falling time) and from“ white”to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.

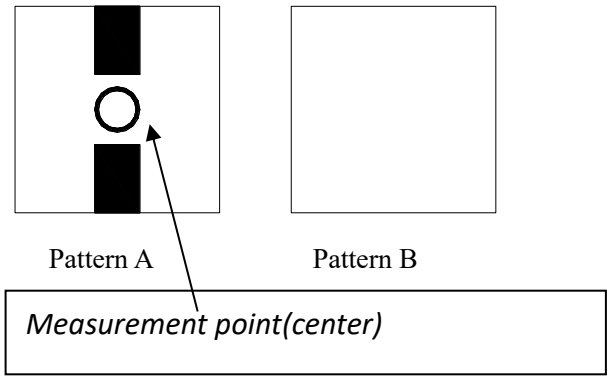


Color gamut:

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 7: Definition of cross talk.

Cross talk ratio(%)=|pattern A Brightness-pattern B Brightness|/pattern A Brightness*100



Electric volume value=3F+/-3Hex

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8. Reliability Test Items and Criteria

No	Test Item	Test condition	Criterion
1	High Temperature Storage	80℃±2℃ 120H Restore 2H at 25℃ Power off	1. After testing, the product only guarantees operation ,but don't guarantee all of the cosmetic specification . 2. Total current
2	Low Temperature Storage	-30℃±2℃ 120H Restore 2H at 25℃ Power off	

3	High Temperature Operation	80℃±2℃ 120H Restore 2H at 25℃ Power on	consumption should not be more than twice of initial value.
4	Low Temperature Operation	-30℃±2℃ 120H Restore 4H at 25℃ Power on	
5	High Temperature/Humidity Operation	60℃±2℃ 90%RH 120H Power on	
6	Temperature Cycle	–30℃←——→80℃ 30min 5min 30min after 50 cycle, Restore 2H at 25℃ Power off	

Note: Operation: Supply 3.3V for logic system.

The inspection terms after reliability test, as below

ITEM	Inspection
Contrast	CR>50%
IDD	IDD<200%
Brightness	Brightness>60%
Color Tone	Color Tone+/-0,05

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause

the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol — Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water — Ketone — Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

Relatively humidity: ≤80%

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

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9.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

10 . Quality Assurance

10.1.Objective

The TFT criteria is set to formalize the TFT quality standards with reference to customer for inspection.

10.2.Scope

The criteria is applicable to all TFT products manufactured by DISEA.

10.3.Tools for Inspection

Tester, calipers, multi-meter, anti-static wrist straps, finger cots, desk Lamps, etc.

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10.4.Sampling Plan and Reference Standards

10.4.1.1 Sampling plan:

Refer to ANSI/ASQZ1.4 NORMAL INSPECTION LEVEL II

AQL:

1) MA=0.65

2) MI=1.0

10.4.1.2 IPC-A-610 Acceptability of Electronic Assemblies.

10.5.Inspection Conditions and Inspection Reference

10.5.1 Cosmetic inspection with naked eyes:

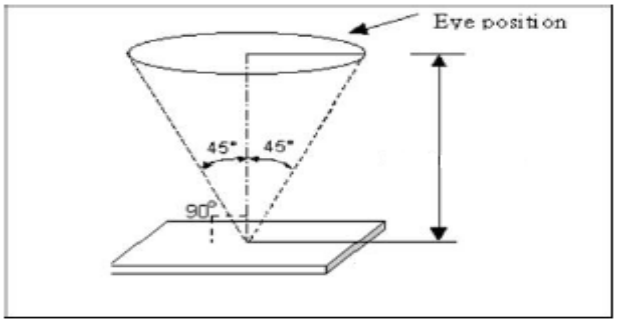
1) Temperature: 25±5℃; relative humidity: 65±20%RH

2) Illumination: Appearance Inspection Condition:600 ~ 800lux;

Operation Inspection Condition: 300lux~500lux

3) Distance: 35cm±5 from the inspector's naked eyes to the LCD panel and inspection time is more than 15s. The ND filter needs to be 20mm away from the LCD surface,and judged at 90° vertical angles.

4) View angle: within 45°from perpendicular to LCM surface (view direction and special parameters refer to production specification).



10.5.2 Definition

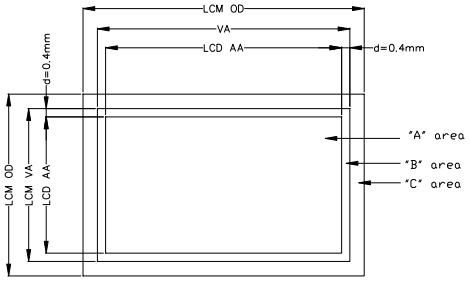
10.5.2.1 Area definition

A area：Active area（AA area）

B area: Viewing area（VA area）

C area: non-view area (out of B area)

10.5.2.2 Any cosmetic defect which do not affect product quality and customer assembling in C area, it's Acceptable. (The dimension is defined on the drawing below)



10.5.2.3 Test condition: refer to product specification

10.5.3 Defect type：

10.5.3.1 A and B area defect type：

Line defect（scratch, soft flocks, fibre）、dot defect（white dot, black dot, same color dot, different color dot, bubble）, stain, pin-hole, light leak, scratch.

10.5.3.2 C area defect type：

Broken, crack/chipping

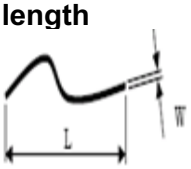
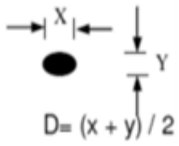
10.5.4 Undefined items or other special items, refer to mutual agreement and limited sample by customer.

10.5.5 Test condition: refer to product specification.

10.6.Defects and Acceptance Standards

10.6.1 Appearance inspection

10.6.1.1 Dot/line defect

Defect	Criterion	Accepted standard	MAJ	MIN
Line defect(foreign objects etc) **W:width** **L:length** 	W≤0.03mm	Accept		√
	0.03mm＜W≤0.05mm, L≤3mm quantity≤1	Accept		√
	W＞0.05mm L＞3mm	Reject		√
Dot defect **(foreign objects etc)** **D:Diameter** 	D≤0.1mm	Accept		√
	0.1mm<D≤0.25mm quantity≤2 distance＞5mm	Accept		√
	D＞0.25mm	Reject		√

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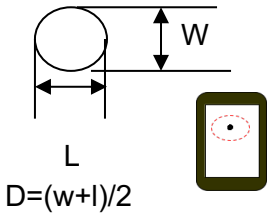
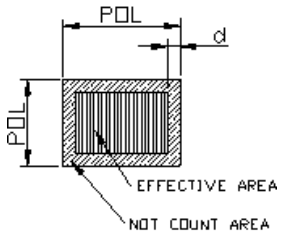
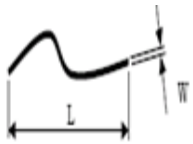
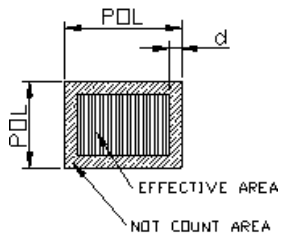
Polarizer with air bubble，convex-concave dots or dent defect in EFECTIVE AREA  D=(w+l)/2 	D≤0.1mm(d=0.4)	Accept		√
	0.1mm<D≤0.25mm (d=0.4) quantity≤2 distance＞5mm	Accept		√
	D＞0.25mm (d=0.4)	Reject		√
Polarizer Line defect in EFECTIVE AREA  	W≤0.03mm(d=0.4)	Accept		√
	0.03mm＜W≤0.05mm, L≤3mm(d=0.4) quantity≤1	Accept		
	W＞0.05mm(d=0.4) L＞3mm(d=0.4)	Reject		

10.6.1.2 Chip and Crack

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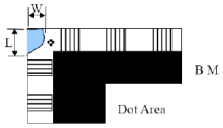
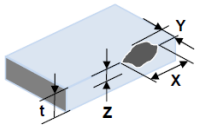
Defect	Criterion	Accepted standard	MAJ	MIN
Broken corners of glass 	ITO Align Mark in LCD is OK. W≤1.5mm,L≤5mm	Accept		
Broken edges of glass 	Y≤2.0mm,X≤5.0mm.Z≤t			
Glass scratch	Not affect ITO line, Judge by dot, line standard 10.6.1.1	Accept		√
	Affect ITO line and be visual.	Reject		√
Glass crack 	Glass crack.	Reject		√

10.6.1.3 Attaching defect（kapton tape/protective film）

Defect	Description	Accepted standard	MAJ	MIN
Protective film	scratch、attaching flat、no shifting	Accept		√
PCBA	Appearance defect	Accept		√
COF	Appearance defect	Accept		√
Silicone spread	Appearance defect	Accept		√
Label for Kapton	Damaged and the text invisible	Reject		√

10.6.2 TFT defects and Inspection Criterion

10.6.2.1 Function items

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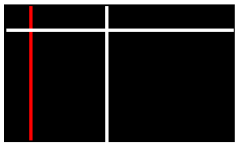
Defects	Inspection Criterion	Pictures	Inspection method/tools	Defect category
No display /function	shows no picture/display in normal connected situation. ->Rejected		Naked eyes/ testers	MA
Missing segment	Shows missing lines in normal display.->Rejected		Naked eyes/ testers	MA
Display abnormal	Not accepted		Naked eyes/ testers	MA
Display dim/bright	Refer to bright value definition	/	Naked eyes/ BM-7	MA
Contrast	Refer to SPEC	/	Naked eyes/ BM-7	MA

10.6.2.2 LCD pixel defect(defect category：MI)

Item	Acceptable count
Area	AA
Bright dots	N≤1
Bright dot-2 adjacent	N≤0
Bright dot-3 adjacent	N≤0
Dark dots	N≤2
Dark dots-2 adjacent	N≤1
Dark dots-3 adjacent	N≤0
Dark or bright dots-3 and more adjacent	N≤0
Total bright and dark dots	N≤3
Minimum distance between bright or dark dots	5mm
Micro bright dots(invisible through 5% ND filter)	D≤0.1mm Accept 0.1mm<D≤0.25mm, N≤2 distance＞5mm
Display Mura or Cross-talk	There should not be invisible through 5%ND filter under 50% gray pattern.

Remark：

1) The definition of dot:

The size of a defective dot over 1/2 of whole sub-pixel is regarded as one defective dot.

2) Bright dot：

Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. The bright dot defect must be visible through 5% ND filter.

3) Dark dot:

Dots appear dark and unchanged in size in which LCD panel is displaying under pure Red,Green,Blue pattern.

4)dots-adjacent

END

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